UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/882,540	06/15/2001	Frido Garritsen	3935P012	8278

7590 06/07/2005

Glenn E. Von Tersch
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1026

EXAMINER	
CAO, CHUN	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 06/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/882,540	GARRITSEN ET AL.	
	Examiner	Art Unit	
	Chun Cao	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Final Rejection

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment Dated 3/21/05.

2. Claims 1 and 3-36 are presented for examination.

3. The text of those applicable section of Title 35, U.S. Code not included in this action can be found in the prior Office Action.

4. The rejections are respectfully maintained and reproduced infra for applicant's convenience.

5. Claims 1, 3, 8-11, 13-15, 18 and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Parrish (Parrish), U.S. patent no. 6,704,879.

As per claim 1, Parrish teaches a method of managing power in a graphics controller [col. 1, lines 35-37], comprising:

receiving a change indication related to a system power supply [col. 2, lines 49-50];

adjusting a first clock [col. 2, lines 49-50];

adjusting a controller power supply voltage [col. 2, lines 60-65] and

informing by the graphics controller a BIOS with an indication of a change related to the system power supply, wherein the informing includes requesting a set of one or more available clock rates [col. 2, line 58-col. 3, line 3; col. 4, lines 31-36].

As per claim 3, Parrish teaches the method further comprises:

receiving the set of one or more available clock rates; checking a state of the graphics controller; choosing a desired clock rate from the set of available

clock rates; adjusting a second clock to conform to the desired clock rate [col. 3, lines 1-18]; and wherein:

adjusting the first clock comprises reducing a rate of the first clock; and adjusting the controller power supply voltage comprises reducing the controller power supply voltage [col. 2, line 58-col. 3, line 18].

As per claim 8, Parrish teaches that the controller power supply voltage is associated with a controller power supply internal to the graphics controller [fig. 1; col. 2, lines 58-65].

As per claim 9, Parrish teaches that the controller power supply voltage is associated with a controller power supply external to the graphics controller, and adjusting the controller power supply voltage includes programming the controller power supply with a signal [fig. 1; col. 2, line 58 –65].

As per claim 10, Parrish teaches of adjusting the first clock comprises increasing a rate of the first clock; and adjusting the controller power supply voltage comprises increasing the controller power supply voltage [col. 2, lines 38-45, 58 –65].

As per claim 11, Parrish teaches of increasing a clock rate of a second clock [col. 2, lines 38-45].

As per claim 13, Parrish teaches of detecting a change related to a system power supply [col. 2, lines 58-65].

As per claim 14, Parrish teaches of installing a software routine [BIOS routines] in a system containing the graphics controller, the software routine

suitable for detecting the change related to the system power supply [col. 1, lines 40-43; col. 2, line 48-65].

As per claim 15 is written in means plus function and contained the same limitations as claims 1 and 3, therefore same rejection is applied.

As per claim 18, Parrish teaches of receiving a software routine suitable for notifying the graphics controller; wherein, notifying the graphics controller comprises executing the software routine [col. 1, lines 40-43; col. 2, line 48-65].

As per claim 19, Parrish teaches of programming the set of available clock frequencies and storing the set of the available clock frequencies in a VGA BIOS [fig. 1; col. 2, line 48-col. 3, line 18].

6. Claims 4, 5 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parrish (Parrish), U.S. patent no. 6,704,879 in view of Dunki-Jacobs et al. (Jacobs), U.S. patent no. 5,349,525.

As per claim 4, Parrish does not explicitly teach of disabling a CLUT.

However, Jacobs teaches of disabling a CLUT [col. 14, lines 27-42].

It would have been obvious to one of ordinary skill in the art at time the invention to Jacobs state above would increase the power consumption of Parrish's system by disabling a CLUT.

As per claim 5, Jacobs teaches of disabling the CLUT [col. 14, lines 27-42]; and Parrish teaches of checking the state of the graphics controller [col. 3, lines 58-65].

As per claim 12, Jacobs teaches of enabling a CLUT [col. 14, lines 27-42].

7. Claims 6, 7, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parrish (Parrish), U.S. patent no. 6,704,879 in view of Powell (Powell), US Pat No. 6,618,042.

As to claims 6 and 16-17, Parrish does not explicitly teach notifying a system to reduce brightness of display.

Powell teaches notifying a system to reduce brightness of display [col. 4, lines

1-8].

It would have been obvious to one of ordinary skill in the art to modify the teachings of Parrish and Powell to notify a system to reducing brightness of a display in order to conserve power.

As per claim 7, Parrish inherently teaches notifying a system comprises notifying a chipset directly [fig. 1; col. 2, lines 58-63].

8. Claims 20-22 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parrish (Parrish), U.S. patent no. 6,704,879 in view of Suboh (Suboh), US Patent No. 5,524,249.

As per claim 20, Parrish does not explicitly teach disabling a first portion of circuitry responsive to checking the state of the graphics controller.

Suboh teaches disabling a first portion of circuitry responsive to checking the state of the graphics controller [col. 4, lines 20-32, 46-48. The PCLK is viewed as a first portion of the circuitry].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Parrish and Suboh to disable a first portion of circuitry in

response to a state of reduced power of a graphics controller in order to conserve power that may be consumed by an enabled portion of circuitry.

As per claim 21, Suboh further teaches disabling a first portion of the circuitry responsive to checking the state of the graphics controller [col. 4, lines 20-32, col. 4 lines 46-48].

As per claim 22, Suboh further teaches enabling the first portion of the graphics controller [col. 8, lines 24-27].

As per claim 36 is written in means plus function and contained the same limitations as claims 1, 3 and 20, therefore same rejection is applied.

9. Claims 23-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parrish (Parrish), U.S. patent no. 6,704,879 in view of Powell (Powell), US Pat No. 6,618,042, Dunki-Jacobs et al. (Jacobs), U.S. patent no. 5,349,525 and Suboh (Suboh), US Patent No. 5,524,249.

As to claims 23-35 basically are the corresponding elements that are carried out the method of operating step in claims 1 and 3-22. Accordingly, claims 23-35 are rejected for the same reason as set forth for claims 1 and 3-22.

Response to Arguments

10. Applicant's arguments filed on 3/21/05, which have been fully considered but they are not persuasive.

11. In the remarks, Applicants argued that 1) Parrish fails to teach, disclose or suggest a limitation of "informing by a graphics controller, a BIOS with an

indication of a change related to the system power supply, wherein the informing includes requesting a set of one or more available clock rate". 2) Parrish fails to teach, disclose or suggest a graphic controller receive power from a power regulator and having a power supply control output.

12. The examiner respectfully traverses the argument for the following reasons:

As to point 1): Parrish teaches of informing by a graphics controller, a BIOS with an indication of a change related to the system power supply [a routine of the graphic BIOS 140 may be invoked to respond the data in the register 115 on the graphics adapter; see col. 2, lines 3-6, 58-65; fig. 1], wherein the informing includes requesting a set of one or more available clock rate [col. 2, lines 58-col. 3, line 3; col. 4, lines 31-36].

As to point 2): inherently, Parrish discloses a graphic controller receive power from a power regulator and having a power supply control output [fig. 1; col. 1, line 64-col. 2, line 3; col. 2, lines 26-45].

Also see detailed rejection indicated above.

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is

filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun Cao whose telephone number is 571-272-3664. The examiner can normally be reached on Monday-Friday from 7:30 am-4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chun Cao

May 31, 2005